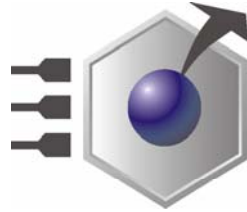


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An0045

CPU-1450; ISA Bus BIOS Settings

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ABOUT THIS MANUAL

This application note contains information about the BIOS menu settings for the ISA Bus of the CPU-1450 to allow user interfacing with ISA cards.



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Conventions

The following table lists conventions used throughout this guide.

Icon	Notice Type	Description
	Information note	Important features or instructions
	Warning	Information to alert you to potential damage to a program, system or device or potential personal injury

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Chapter 1 CPU-1450 ISA Bus

This application note is intended to explain how to properly setup the CPU-1450 BIOS settings in order to open the IO space on the ISA bus to allow users to interface with external ISA devices connected to the PC104 bus.

CPU-1450 ISA Architecture

The CPU-1450 ISA bus is based on an ITE IT8888F chipset, which is a PCI to ISA bridge single function device. The IT8888F serves as a bridge between the PCI bus and ISA bus. The ISA parallel IRQ and IOCHCK# are serialized on the SIRQ lines. The device includes an ISA interface, which supports ISA compatible functions. Figure 1 shows the IT8888F IC Block Diagram. For detailed information please refer to the component data sheet.

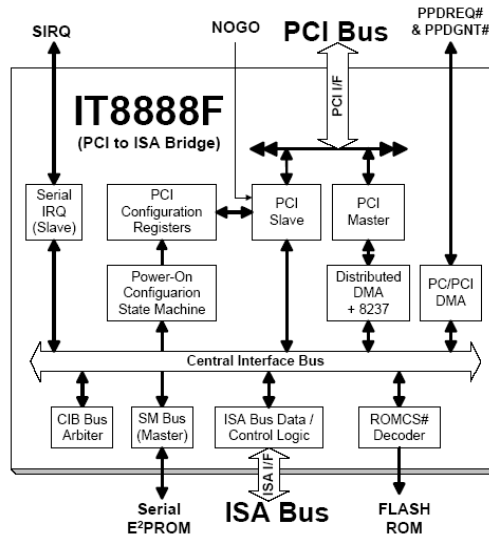


Figure 1. IT8888F IC Block Diagram

BIOS Settings

The user can easily configure the ITE IT8888F chipset with the user-friendly ISA Bus BIOS configuration mask added to the BIOS setup. Figure 2 shows the BIOS mask for the ISA Bus, which may be accessed by entering the BIOS as described in the CPU's user manual.

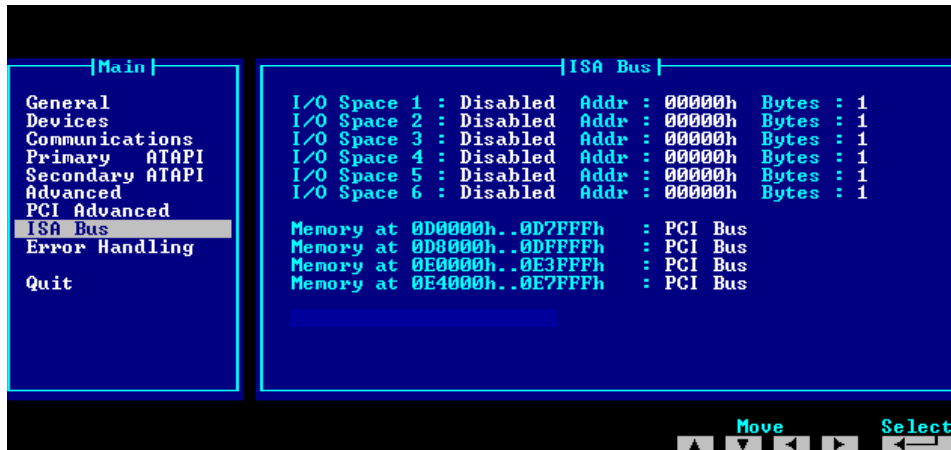


Figure 2. ISA Bus BIOS mask

The ISA Bus BIOS mask is divided into two main sections:

- I/O Space (Enable/Disable, Addr, and Bytes)
- Memory Space

I/O Space

It is possible to enable six different I/O spaces. In order to do so, you must declare the I/O address and the number of bytes required for the peripheral. Typically the I/O address is the base address of the peripheral device connected to the ISA bus. The required bytes entry is typically the contiguous I/O space reserved for the peripheral.

Typical values are listed below:

Addr: XXXXXh (user entry)
 Bytes: 1, 2, 4, 8, 16, 32, 64 and 128

Memory Space

There are four memory areas available to be assigned for the ISA bus and are listed below:

Memory at 0D0000h .. 0D7FFFh
 Memory at 0D8000h .. 0DFFFFh
 Memory at 0E0000h .. 0E3FFFh
 Memory at 0E4000h .. 0E7FFFh

User can assign the above memory spaces to the PCI bus or to the ISA bus depending on the ISA peripheral memory requirements.

External Floppy and Video controllers

CPU-1450 BIOS integrates an automatic detection of external floppy controller cards and automatically reserves the IO space and the memory map for those resources.



If you use an external floppy controller the I/O Space 6 is automatically reserved from BIOS to map the following I/O resources:

I/O Space 6 Addr : 3F0h Bytes : 8 ; I/O floppy controller from 3F0h to 3F7h.

Note that the BIOS doesn't automatically fill the I/O Space 6 field unless an external floppy is connected.

Mechanical requirements

The ISA and PCI buses on the CPU-1450 are only installed on the bottom of the board because the top is occupied by a heatsink. In order to interface the CPU-1450 with another PC/104 board, the CPU must be placed on top of the stack.

A module without a PC/104+ (PCI) bus may have components mechanically interfering with the extruding connector of a PC/104+ module (e.g. CPU-1450). If this is the case a height adapter must be installed on the PC/104 bus to prevent mechanical interferences between the PC/104+ (PCI) bus and the components included on the adjacent module.

Chapter 2 Practical Examples



To give you a detailed explanation we propose some practical examples regarding the interfacing of some Eurotech ISA boards and the CPU-1450, showing the necessary BIOS settings.

INT-1250 and CPU-1450

We first refer to the interface of an INT-1250 (a PC/104 Sound Blaster and Windows Sound System compatible audio module) with the CPU-1450. We set the proper ISA bus BIOS setup parameters and enable the IO space for the INT-1250 sound blaster pnp board. Refer to the INT-1250 user manual for detailed information.

1. Enter the CPU-1450 BIOS menu pressing F2 key during boot-up and select the ISA Bus Menu.
2. Move between the I/O Space enabling the the following ISA I/O space entries:

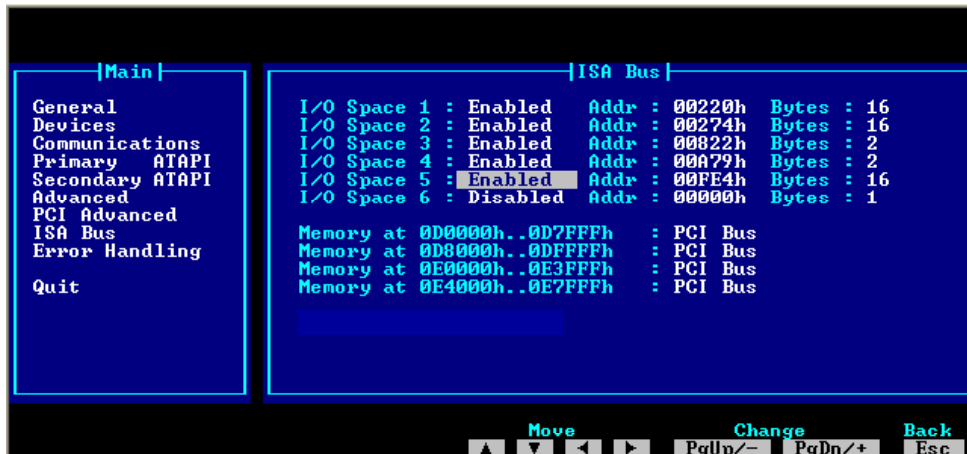


Figure 3. ISA Bus settings for INT-1250

The 00279h and 00A79h address are required for INT-1250 plug and play capabilities. Note that the INT-1250 board doesn't require ISA memory space (now available for the PCI bus).

3. Quit BIOS saving data to flash.
4. Now run your preferred O.S. (in our case we used Win XP Pro). If your Windows XP hasn't detected the board, perform a search using Device Manager to scan for new hardware devices.
5. The board should be found. If not, or if a yellow exclamation mark appears, finish the configuration manually, entering the proper parameter settings exactly as you programmed into the BIOS ISA Bus menu.
6. Try your audio functions and enjoy your music! If no audio is produced from the board make sure the DMA is proper configured for ISA bus.

COM-1270 and CPU-1450

This second example is intended to describe the ISA Bus BIOS configuration to make the COM-1270 interface properly with the CPU-1450.

The COM-1270 is a PC/104 module with 8 serial ports (RS232 or RS422/485), 2 TTL CAN ctrls, 16 digital I/O, and Ethernet (TP and AUI). This example is interesting because of the high number of ISA peripherals present on the board and because of the CAN memory resources necessary.

Before starting, we suggest to refer to the COM-1270 user manual to obtain further information regarding the hardware functionalities of the COM-1270 and to verify how to setup board parameters for custom user configuration.

We've listed on the following table the COM-1270 parameters that we've initialized on the COM-1270 EEPROM for our specific configuration:

IO Space	Bytes	Offset	Description
150h	8 bytes	150h - 157h	COM-1270 IO Address selection
220h	32 bytes	220h – 240h	RTL8019 Ethernet
280h	8bytes*8serial ports	280h – 2BFh	Serial Ports Base Address
2C0h	1 byte	2C0h	IRQ Vector
D8000h	256 bytes	D8000h – D80FFh	CAN1 Interface Base Address
D8000h	256 bytes	D8100h – D81FFh	CAN2 Interface Base Address

Table 1. COM-1270 board parameters

1. Enter the CPU-1450 BIOS menù pressing F2 key at boot time and select the ISA Bus Menu
2. Move between the I/O Space enabling the the following ISA I/O space entries:

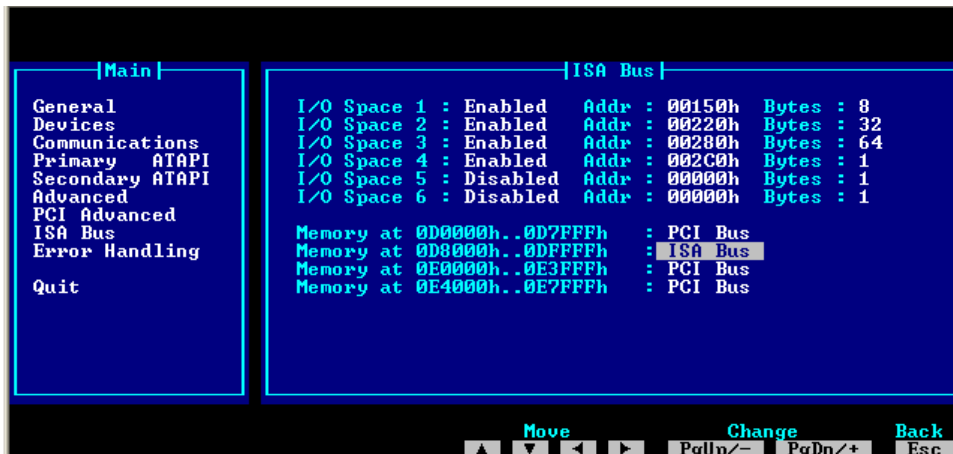


Figure 4. ISA Bus settings for COM-1270

3. Quit BIOS setup saving data to flash.
4. Launch the COM-1270 SETUP.EXE (for detailed information on this please refer to the COM-1270 user's manual). Note that first to launch the COM-1270 setup utility we've configured the BIOS ISA Bus parameters to allow setup utility detecting the COM-1270 module otherwise SETUP program fails detecting COM-1270 module and setup couldn't store data to EEPROM.

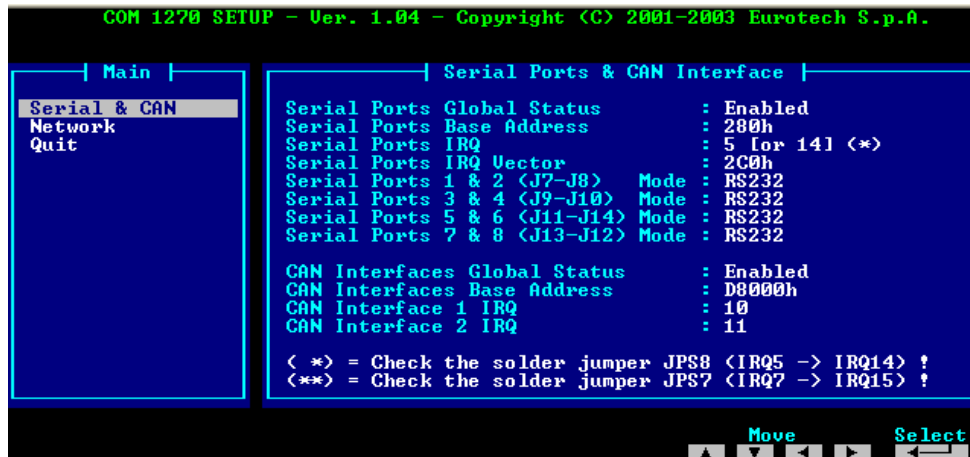


Figure 5. COM-1270 Setup program Serial & CAN

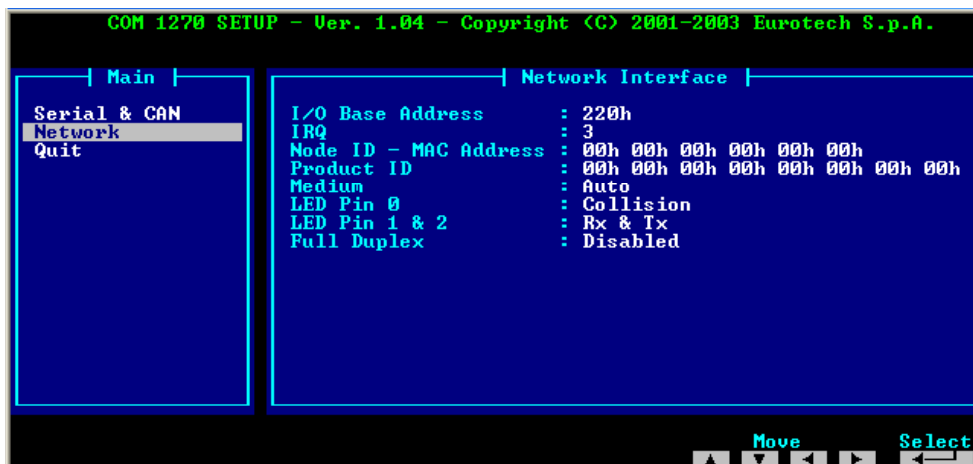


Figure 6. COM-1270 Setup program Network

Here some considerations related to the COM-1270 IO map:

- The COM-1270 board can be accessed via four IO Address which may be selected with JP1 and JP2 jumpers between the following addresses: 110h, **150h**, 1A0h and 1E0h. The I/O BIOS ISA Bus has been initialized with the default address opening 8 bytes locations.
 - The COM-1270 user's manual reports a list of the selectable I/O base address for the serial ports. Those are 180h, 1C0h, 200h, 240h, **280h**, 2C0h, 300h, 340h, 380h and 3C0h. We used the default one. Note that if you use different I/O base address you've to modify the BIOS ISA Bus configuration, the 64 bytes location remain the same for 8 serials ports.
 - The CPU-1450 ISA Bus BIOS menu doesn't allow user to select all the possible CAN I/O base address listed on the COM-1270 user's manual but only a subset of this.
 - The COM-1270's network interface is based on a Realtech RTL8019 chipset. This may be addressed in the range of 220h to 3E0h with steps of 20h. The factory default is 220h. Pay attention: the Realtech RTL8019 may be configured with the RTL8019 utility program, allowing you to configure the chip as JumperLess or as a pnp device. By factory default, the COM-1270 is shipped with the JumperLess option enabled. If you intend to use the CPU-1450 in conjunction with the RTL8019 chipset you need to verify the default option.
5. At this point you can run your application verifying that all the resources are accessible and available.

Related Documents

For more information please refer to the specific CPU user manual.
IT8888F Data Sheet - PCI-to-ISA Bridge Chip
INT-1250 user's manual
COM-1270 user's manual

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