Quality fanless computers

FACET Cards

Design Guide

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CompuLab Ltd.
17 HaYetsira St., Yokneam Elite 20692,
P.O.B 687
ISRAEL
Tel: +972-4-8290100
http://www.compulab.co.il
http://fit-pc.com/web/
Fax: +972-4-8325251

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Revision History

Revision	Author/Engineer	Revision Changes
0.99	Maxim Birger	Preliminary release
1.0	Maxim Birger	Initial public release

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1 Introduction

1.1 About This Document

This document is part of a set of reference documentation necessary to design and program custom FACET Cards for fitlet computers.

1.2 Related Documents

Document	Link
PCI express mini card electromechanical specification 1.2	http://fit-pc.com/download/facet-cards/documents/PCI_Express_miniCard_Electromechanical_specs_rev1.2.pdf
FACET Cards Wiki	http://www.fit-pc.com/wiki/index.php/Fit-PC_Product_Line:FACET_Modules
FACET FC-LAN reference card	http://www.fit-pc.com/wiki/index.php/FACET_Cards:FC-LAN_Card
FACET FC-LAN schematics design	http://fit-pc.com/download/facet-cards/fc-lan/FC-LAN-V1_0-Schematics.zip
FACET FC-LAN layout design	http://fit-pc.com/download/facet-cards/fc-lan/FC-LAN-V1_0-Layout.zip
FACET FC-LAN mechanical file	http://fit-pc.com/download/facet-cards/fc-lan/FC-LAN-V1_0-Mechanical.zip
FACET FC-LAN assembly file	http://fit-pc.com/download/facet-cards/fc-lan/FC-LAN-V1_0-Assembly-drawings.zip

2 Overview

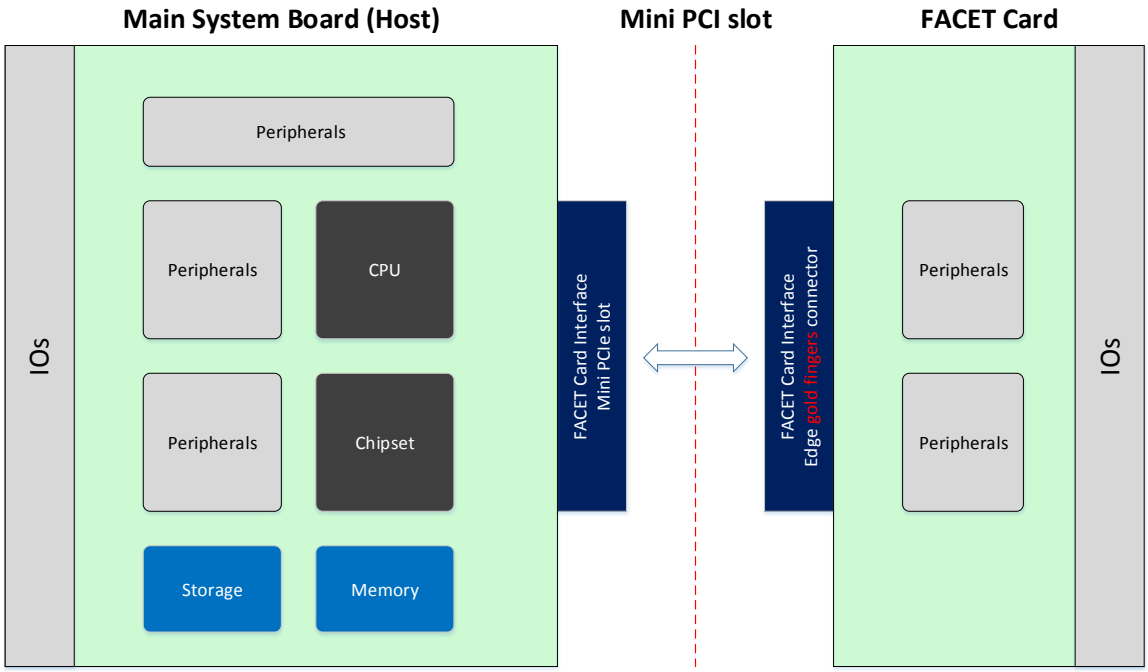
2.1 Scope

FACET Card (**F**unction **A**nd **C**onnectivity **E**xtension **T**-Card) serve as optional extension board providing additional peripherals and IO connectivity options for ***fitlet*** products. This document outlines FACET Card interface specification and custom FACET Card design guidelines, requirements and recommendations.

2.2 Concept

FACET Cards are implemented with internal T-shaped extension board. The extension board is connected to already available motherboard's mini PCI Express slot, featuring standard PC interfaces such as PCIe, USB2, SMBus and LPC Bus.

Figure 1 – FACET Card Concept



3 FACET Interface

3.1.1 FACET Electrical Interface

FACET Electrical interface provided in the table below:

Table 1 – Mini PCI Express edge connector pinout

mini PCI Express edge connector					
Pin #	**Pin Name**	**Signal Description**	**Pin #**	**Pin Name**	**Signal Description**
1	WAKE#	Open drain, active low signal driven low by a mini PCIe card to reactivate the PCIe link	2	3.3Vaux	3.3V power rail
3	PERn2		4	GND	Ground connection
5	PERp2	PCI Express Gen2 differential receive pair 2	6	1.5V	1.5V power rail
7	CLKREQ#	Clock request - open drain, active low driven by mini PCIe card to request PCIe reference clock	8	LAD0	LPC Bus Data signals
9	GND	Ground connection	10	LAD1	
11	REFCLK-	Reference clock used to assist the synchronization of PCI Express interface timing circuits	12	LAD2	
13	REFCLK+		14	LAD3	
15	GND	Ground connection	16	LFRAME#	LPC Bus frame signal. Active Low.
Mechanical Notch Key					
17	PETn2		18	GND	Ground connection
19	PETp2	PCI Express Gen2 differential transmit pair 2	20	MPCIE0_DIS# / W_DISABLE#	Active low signal when asserted by the system disable PCIE/radio operation.
21	GND	Ground connection	22	PERST#	Asserted when power is switched off and also can be used by the system to force HW reset
23	PERn0		24	3.3Vaux	3.3V power rail
25	PERp0	PCI Express Gen2 differential receive pair 0	26	GND	Ground connection
27	GND	Ground connection	28	1.5V	1.5V power rail
29	GND	Ground connection	30	SMB_CLK	Optional SMBus two-wire interface for Host/mini PCIe module communication
31	PETn0		32	SMB_DATA	
33	PETp0	PCI Express Gen2 differential transmit pair 0	34	GND	Ground connection
35	GND	Ground connection	36	USB_D-	USB Host Interface
37	LPC_CLK0	LPC Bus clock	38	USB_D+	
39	3.3Vaux	3.3V power rail	40	GND	Ground connection
41	3.3Vaux	3.3V power rail	42	LED_WWAN#/ LPC_SMI#	Active low output signals are provided to allow status indications to users via system provided LEDs (or LPC Bus control signals).
43	PETn1		44	LED_WLAN#/ LPC_PME#	
45	PETp1	PCI Express Gen2 differential transmit pair 1	46	LED_WPAN#/ SERIRQ	
47	LPC_RST#	LPC Bus Reset signal. Active Low.	48	1.5V	1.5V power rail
49	PERn1		50	GND	Ground connection
51	PERp1	PCI Express Gen2 differential receive pair 1	52	3.3Vaux	3.3V power rail

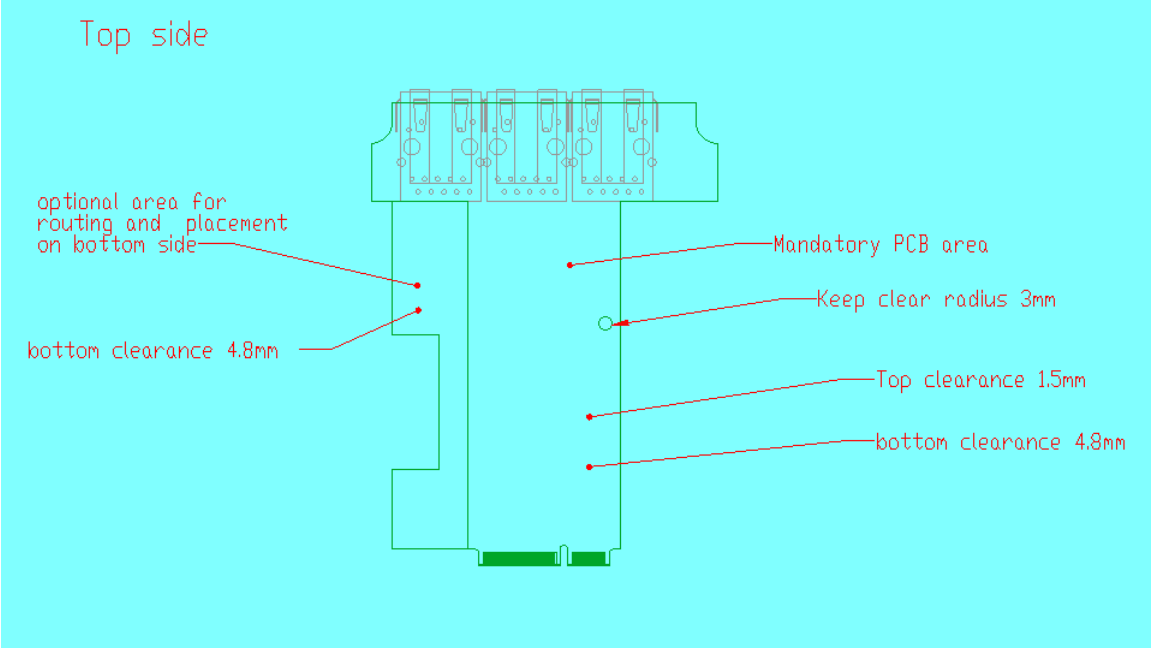
FACET Card interface based on regular mini PCI Express interface featuring extended signals and functionality, as legacy LPC Bus interface and additional PCI Express lanes.

3.1.2 FACET Mechanical Interface

As noted in the previous section, FACET interface based on standard mini PCI express connection, electrical as well as mechanical, meaning all mechanical and layout guidelines apply for FACET mechanical design.

PCB shape of custom FACET derived from fitlet-X PCB design, mechanical stack-up and other mechanical constraints, shown in the DXF file below. The file can be downloaded from product wiki portal.

Figure 2 – FACET LAN DXF file



FACET PCB design should meet mini PCI Express design guidelines in terms of edge connector design (hard gold fingers), PCB thickness, other parameters, and follow general recommendations described in PCI express mini card electromechanical specification 1.2.

4 Extended Functionality

4.1 PCI Express Interface

Fitlet-X SoC provides several PCI Express Root Ports, supporting the PCI Express Base Specification, Revision 2.0. Each Root Port lane supports up to 5 Gbps bandwidth in each direction (10 Gbps concurrent). FACET PCI Express interface consist of 3x PCI Express gen2.0 lanes.

4.2 LPC Bus Interface

The Low Pin Count (LPC) bus interface is a cost-efficient, low-speed interface designed to support low-speed legacy (ISA, X-bus) devices. The LPC interface essentially eliminates the need of ISA and X-bus in the system. Here the ISA bus is internal to SoC and is used for connecting to the legacy Direct Memory Access (DMA) logic. The LPC host controller is integrated into the SoC. It connects to the internal A-Link bus on one side and the LPC and Serial Peripheral Interface (SPI) buses on the other side. The ISA interface is only used for legacy DMA operation.

Examples of LPC devices include Super I/O (disk controller, keyboard controller), BIOS RAM, audio, Trusted Platform Module (TPM), and system management controller.

LPC host controller has the A-Link bus on one side and the LPC bus on the other. The host controller supports memory and I/O read/write, DMA read/write, and bus master memory I/O read/write. It supports up to two bus masters and seven DMA channels.