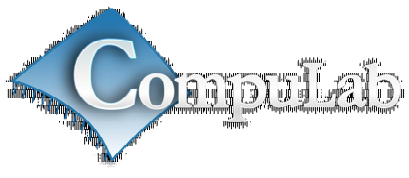
SBC-FITPC3

Reference Guide



CompuLab
P.O. Box 687 Yokneam Elite
20692 ISRAEL
Tel: +972 (4) 8290100
http://www.compulab.co.il
Fax: +972 (4) 8290126

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Table 1 Document Revision Notes

Date	Description
December 2011	• First release

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents necessary to operate and program CompuLab Fit-PC3.

1.2 Related Documents

For additional information not covered in this manual, please refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
Fit-PC3 Resources	http://www.fitpc.com

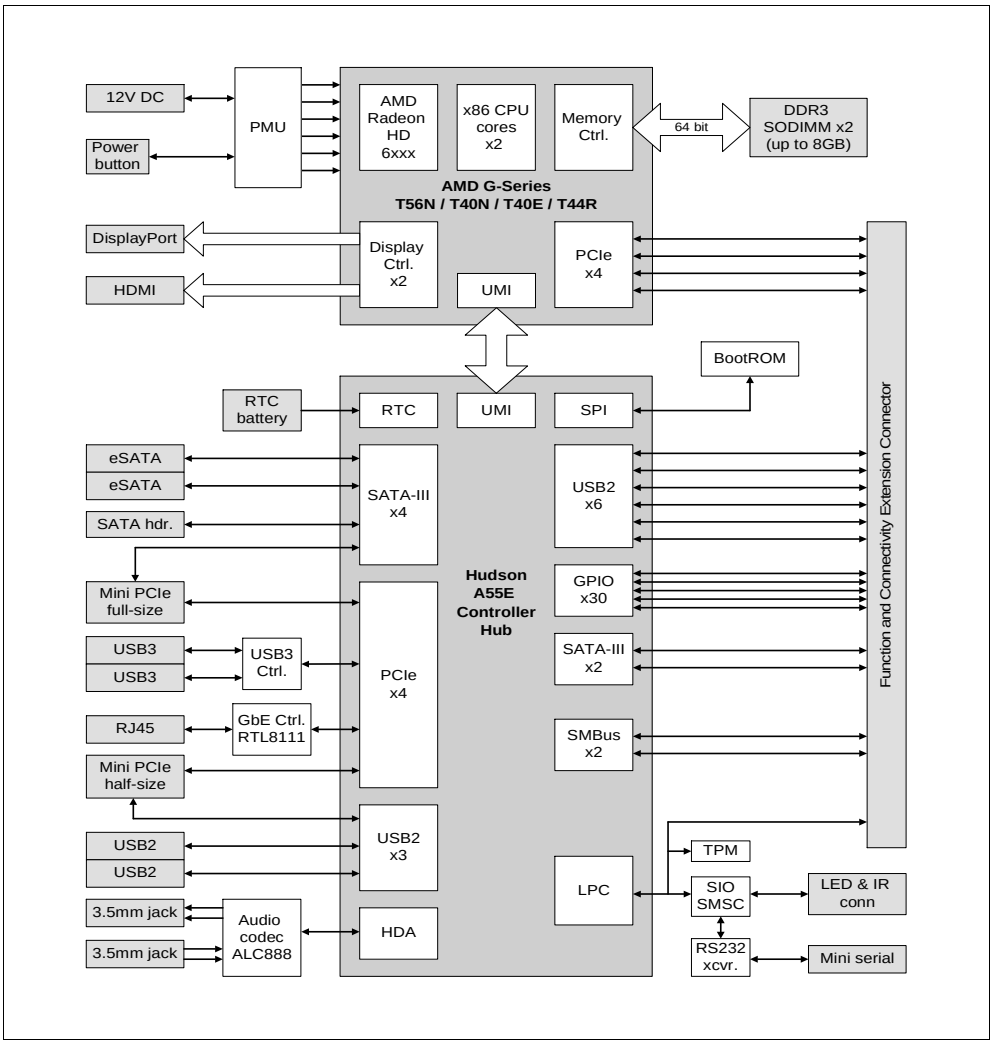
2 OVERVIEW

2.1 Highlights

Fit-PC3 is a fan-less, extensible PC with powerful multimedia capabilities, based on AMD embedded G-Series platform.

2.2 Block Diagram

Figure 1 SBC-FITPC3 Block Diagram



2.3 Features

System

Feature	Specifications				Notes
CPU	AMD G-T44R 64bit single core 1GHz 9W TDP	AMD G-T40N 64bit dual core 1GHz 9W TDP	AMD G-T40E 64bit single core 1GHz 6.4W TDP	AMD G-T56N 64bit dual core 1.65GHz 18W TDP	
RAM	Up to 8 GB, DDR3, 1333 MHz, 64-bit (two SO-DIMM sockets)				Configurable
Storage	Internal 2.5” hard drive interface				
	Two eSATA ports, up to 6 Gbit/s				
	mSATA (multiplexed with full-size mini PCIe socket)				

Graphics

Feature	Specifications				Notes
GPU	AMD G-T44R	AMD G-T40N	AMD G-T40E	AMD G-T56N	
	Radeon HD 6250	Radeon HD 6290	Radeon HD 6250	Radeon HD 6320	
HDMI	HDMI 1.3a up to 1920x1200 at 60 Hz			HDMI 1.4a up to 1920x1200 at 60 Hz	
HDMI Stereo 3D	-	-	-	+	
DisplayPort	Up to 2560x1600 at 60Hz				

I/O

Feature	Specifications	Notes
Audio	Stereo line-out and stereo line-in	
	7.1 channel S/PDIF, (electrical through 3.5mm jack)	
Network	1000 BaseT Ethernet port, activity LEDs, RJ-45 connector	
	802.11b/g/n Wi-Fi, 2 antennas, 150 Mbit/s	Optional Mini PCIe module
	Bluetooth V3.0 + EDR	
USB	Two USB 3.0 host ports, 5 Gbit/s	
	Two USB 2.0 host ports, 480 Mbit/s	
	Four additional USB 2.0 host ports, 480 Mbit/s (front panel)	Optional module
RS232	Partial modem controls, ultra mini serial connector	
IR	Consumer IR receiver	
Expansion	Mini PCIe socket, half-size (used for wireless module)	
	Mini PCIe socket, full-size, with mSATA support	
	Proprietary FACE Module (Function And Connectivity Extension Module) • 4x PCIe • 6x USB2 • 2x SATA • 4x SMBus • 30x GPIOs • LPC	

Electrical and Mechanical

Feature	Specifications				Notes
Power Supply	Unregulated 10 to 16 volt input				
Power consumption	AMD G-T44R	AMD G-T40N	AMD G-T40E	AMD G-T56N	Depends on system load
	TBD	8W – 17W	7W – 15W	9W – 24W	
Dimensions	16cm x 16cm x 2.5cm			19cm x 16cm x 4cm	

3 CORE SYSTEM COMPONENTS

3.1 AMD Embedded G-Series APU

3.1.1 CPU Core

The AMD embedded G-Series APU x86 core supports the following key features:

- Single or dual x86 Processor
- AMD64 64-bit ISA
- Advanced Branch Prediction
- Out-of-Order Instruction Execution
- 64-bit floating-point unit
- SSE1,2,3, SSSE3 ISA, SSE4A, MMX
- AMD Virtualization technology

3.1.2 GPU Core

The AMD embedded G-Series APU integrated GPU core supports the following key features:

- Dedicated graphics memory controller
  - High efficiency ring bus memory controller
  - Direct connection to memory
- 2D Acceleration
  - Highly-optimized 128-bit engine, capable of processing multiple pixels per clock
- 3D Acceleration
  - Full DirectX 11 support, including full speed 32-bit floating point per component operations
  - Shader Model 5
  - OpenCL 1.1 support
  - OpenGL 4.0 support
- Motion Video Acceleration
  - Dedicated hardware (UVD 3) for H.264, VC-1 and MPEG2 decode
  - HD HQV and SD HQV support: noise removal, detail enhancement, color enhancement, cadence detection, sharpness, and advanced de-interlacing
  - Super up-conversion for SD to HD resolutions

3.2 System Memory

3.2.1 DRAM

The Fit-PC3 features two user accessible DDR3 SO-DIMM sockets. The DRAM interface is 64-bits wide and runs at a 666 MHz clock. Fit-PC3 supports up to 8GB of memory.

3.3 Display Subsystem

3.3.1 HDMI

The Fit-PC3 HDMI output is implemented with the APU HDMI interface. HDMI signals are routed to the display output connector P13. The HDMI output supports resolutions of up to 1920 x 1200 at 60Hz.

NOTE: HDMI 1.4a is supported only in the Fit-PC3 model featuring the G-T56N APU. Other Fit-PC3 models support HDMI 1.3a.

3.3.2 DisplayPort

The Fit-PC3 DisplayPort output is implemented with the APU DisplayPort interface. DisplayPort signals are routed to the display output connector P19. The DisplayPort output supports resolutions of up to 2560 x 1600 at 60Hz.

3.4 Audio Subsystem

The Fit-PC3 audio subsystem is implemented with the Realtek ALC888S-VC2 audio codec. The ALC888S-VC2 is a high performance 7.1+2 channel high definition audio codec with an independent S/PDIF output. The codec features ten DAC channels that simultaneously support 7.1 sound playback and an independent stereo output.

The audio codec is connected to the A55E Controller Hub HDA port.

The ALC888S-VC2 supports the following main features:

- Meets premium audio requirements for Microsoft WLP 3.10
- Meets stricter performance requirements for future WLP effective from 01 June 2008
- High-performance DACs with 97dB SNR (A-Weighting), ADCs with 90dB SNR (A-Weighting)
- Ten DAC channels support 16/20/24-bit PCM format for 7.1 sound playback, plus 2 channels of independent stereo sound output (multiple streaming) through the front panel output
- Two stereo ADCs support 16/20/24-bit PCM format recording simultaneously
- All DACs supports 16/20/24-bit, 44.1k/48k/96k/192kHz sample rate
- All ADCs supports 16/20/24-btt, 44.1k/48k/96k/192kHz sample rate
- SPDIF-OUT converter supports 16/20/24-bit, 44.1k/48k/88.2k/96k/192kHz sample rate
- SPDIF-IN converter supports 44.1k/48k/96k/192k Hz sample rate
- Wide range (–80dB ~ +42dB) volume control with 1.5dB resolution of analog to analog mixer gain
- Software selectable boost gain (+10/+20/+30dB) for analog microphone input
- Built-in headphone amplifiers for each re-tasking jack
- Integrates high-pass filter to cancel DC offset generated from digital microphone

3.4.1 Analog Audio

The Fit-PC3 analog audio sub-system features a stereo line output and a stereo line input implemented with the ALC888S-VC2 codec.

Analog line output is routed to the audio jack P5. Analog line input is routed to the audio jack P4.

Table 3 Audio Characteristics

Parameter	Min	Typical	Max	Unit
Full-Scale Input Voltage				
All Inputs (gain=0dB)	-	1.6	-	Vrms
ADC	-	1.1	-	Vrms
Full-Scale Output Voltage				
DAC	-	1.4	-	Vrms
Headphone Amplifier Output@32	-	1.6	-	Vrms
S/N (A Weighted)				
ADC	-	90	-	dB FSA
DAC	-	96	-	dB FSA
Headphone Amplifier Output@32	-	95	-	dB FSA
THD+N				
ADC	-	-84	-	dB FS
DAC	-	-90	-	dB FS
Headphone Amplifier Output@32	-	-80	-	dB FS
Frequency Response				
ADC	10	-	0.45*Fs	Hz
DAC	0	-	0.45*Fs	Hz
Power Supply Rejection	-	-50	-	dB
Total Out-of-Band Noise (28.8kHz~100kHz)	-	-60	-	dB
Amplifier Gain Step	-	1.5	-	dB
Crosstalk Between Input Channels	-	-80	-	dB
Input Impedance (gain=0dB)	-	47	-	KΩ
Output Impedance				
Amplified Output	-	1	-	Ω
Non-amplified Output	-	100	-	Ω

3.4.2 S/PDIF Output

The S/PDIF output is implemented with the ALC888S-VC2 codec. SPDIF-OUT converter supports 16/20/24-bit, 44.1k/48k/88.2k/96k/192kHz sample rates. The S/PDIF output signal is routed to audio jack P5.

3.4.3 S/PDIF Input

The S/PDIF input is implemented with the ALC888S-VC2 codec. SPDIF-IN converter supports 44.1k/48k/96k/192kHz sample rates. The S/PDIF input signal is routed to audio jack P4.

3.5 USB3.0 Subsystem

The Fit-PC3 features two external USB3.0 ports that are implemented with the Texas Instruments TUSB7320 host controller. The down-stream ports support SuperSpeed, High-speed and Full-speed/Low-speed connections.

The TUSB7320 host controller is interfaced with the PCIe interface of the A55E Controller Hub. The two USB down-stream ports are routed to the dual-stacked USB connector P8.

For additional details, please refer to the TUSB7320 datasheet, available from http://www.ti.com/.

3.6 Gigabit Ethernet

The Fit-PC3 Gigabit Ethernet interface is implemented with the RTL8111D Realtek Gigabit Ethernet controller. The controller is connected to the PCIe interface of the A55E Controller Hub. The interface supports the following main features:

- Full compliance with IEEE 802.3 standard
- Crossover Detection and Auto-Correction
- Wake-on-LAN and remote wake-up support
- Auto-negotiation
- Activity and speed indicator LED controls

Gigabit Ethernet signals are routed to the RJ-45 connector P12.

3.7 Super I/O

The Fit-PC3 utilizes a SMSC SIO1007 Super I/O controller to implement RS232 and CIR interfaces. The SIO1007 Super I/O controller is interfaced with the A55E controller hub LPC port.

CIR signals are routed to the IR connector U7.

UART signals are routed through the RS232 transceiver to the RS232 connector P2.

4 SYSTEM LOGIC

4.1 Power Subsystem

4.1.1 Power Rails

The Fit-PC3 is powered with a single 12V power supply.

Table 4 Power signals

Signal Name	Type	Description
VIN_12V	P	Main power supply. Typical voltage – 12V.
GND	P	Common ground.

4.1.2 RTC Back-Up Battery

The Fit-PC3 features an on-board 18mAh rechargeable coin cell lithium battery, which maintains the Fit-PC3 RTC when the main power supply is not present. The battery is being re-charged whenever Fit-PC3 is connected to the main power supply. The back-up battery will sustain the RTC for up to 6 months with no charging.

4.1.3 Power-on Logic

The Fit-PC3 is designed to support standard PC power-on logic. The Fit-PC3 BIOS can be configured for the following behavior for when main power is applied:

- Stay off
- Turn on automatically
- Preserve the last state before power disconnect

4.1.4 Power Button

The Fit-PC3 power button SW2 controls the system power state. The button serves as a standard ON/OFF button in a typical PC system. The button behavior is programmable using standard tools available in MS Windows and Linux.

5 FACE MODULE INTERFACES

5.1 PCIe

Table 5 PCIe Interface Signals

Signal Name	Pin #	Type	Description	Notes
PCIe-0				
PCIE_P0_TX_P	PX1-A44	I/O	PCIe port 0 transmit positive	
PCIE_P0_TX_N	PX1-A45	I/O	PCIe port 0 transmit negative	
PCIE_P0_RX_P	PX1-B44	I/O	PCIe port 0 receive positive	
PCIE_P0_RX_N	PX1-B45	I/O	PCIe port 0 receive negative	
PCIe-1				
PCIE_P1_TX_P	PX1-A41	I/O	PCIe port 1 transmit positive	
PCIE_P1_TX_N	PX1-A42	I/O	PCIe port 1 transmit negative	
PCIE_P1_RX_P	PX1-B41	I/O	PCIe port 1 receive positive	
PCIE_P1_RX_N	PX1-B42	I/O	PCIe port 1 receive negative	
PCIe-2				
PCIE_P2_TX_P	PX1-A38	I/O	PCIe port 2 transmit positive	
PCIE_P2_TX_N	PX1-A39	I/O	PCIe port 2 transmit negative	
PCIE_P2_RX_P	PX1-B38	I/O	PCIe port 2 receive positive	
PCIE_P2_RX_N	PX1-B39	I/O	PCIe port 2 receive negative	
PCIe-3				
PCIE_P3_TX_P	PX1-A35	I/O	PCIe port 3 transmit positive	
PCIE_P3_TX N	PX1-A36	I/O	PCIe port 3 transmit negative	
PCIE_P3_RX_P	PX1-B35	I/O	PCIe port 3 receive positive	
PCIE_P3_RX_N	PX1-B36	I/O	PCIe port 3 receive negative	
PCIe generic				
PCIE_CLK1_P	PX1-B32	O	PCIe clock 1 positive	
PCIE_CLK1_N	PX1-B33	O	PCIe clock 1 negative	
PCIE_CLK2_P	PX2-B26	O	PCIe clock 2 positive	
PCIE_CLK2_N	PX2-B27	O	PCIe clock 2 negative	
PCIE_RESET#	PX1-B31	O	PCIe reset. Asserted during transition to S3/S4/S5.	
PCIE_WKUP#	PX1-A37	I	PCIe wake-up	
PCIE_CLKREQ#	PX2-A41	I	PCIe clock request	

5.2 SATA

Table 6 SATA Interface Signals

Signal Name	Pin #	Type	Description	Notes
SATA-1				
SATA_P1_TX_P	PX1-B8	O	SATA channel 1 transmit positive	
SATA_P1_TX_N	PX1-B9	O	SATA channel 1 transmit negative	
SATA_P1_RX_P	PX1-B11	I	SATA channel 1 receive positive	
SATA_P1_RX_N	PX1-B12	I	SATA channel 1 receive negative	
SATA-2				
SATA_P2_TX_P	PX1-A2	O	SATA channel 2 transmit positive	
SATA_P2_TX_N	PX1-A3	O	SATA channel 2 transmit negative	
SATA_P2_RX_P	PX1-A5	I	SATA channel 2 receive positive	
SATA_P2_RX_N	PX1-A6	I	SATA channel 2 receive negative	
SATA-3				
SATA_P3_TX_P	PX1-A8	O	SATA channel 3 transmit positive	
SATA_P3_TX_N	PX1-A9	O	SATA channel 3 transmit negative	
SATA_P3_RX_P	PX1-A11	I	SATA channel 3 receive positive	
SATA_P3_RX_N	PX1-A12	I	SATA channel 3 receive negative	
SATA generic				
SATA_ACT#	PX1-B4	OD	SATA channel active	

5.3 USB

Table 7 PCIe Interface Signals

Signal Name	Pin #	Type	Description	Notes
USB-4				
USB_P4_P	P1-A24	I/O	USB port 4 positive I/O	
USB_P4_N	P1-A25	I/O	USB port 4 negative I/O	
USB-5				
USB_P5_P	PX2-A48	I/O	USB port 5 positive I/O	
USB_P5_N	PX2-A49	I/O	USB port 5 negative I/O	
USB-7				
USB_P7_P	PX1-B17	I/O	USB port 7 positive I/O	
USB_P7_N	PX1-B18	I/O	USB port 7 negative I/O	
USB-8				
USB_P8_P	PX1-B14	I/O	USB port 8 positive I/O	
USB_P8_N	PX1-B15	I/O	USB port 8 negative I/O	
USB-12				
USB_P12_P	PX1-A27	I/O	USB port 12 positive I/O	
USB_P12_N	PX1-A28	I/O	USB port 12 negative I/O	
USB-13				
USB_P13_P	PX2-A45	I/O	USB port 13 positive I/O	
USB_P13_N	PX2-A46	I/O	USB port 13 negative I/O	
USB Overcurrent				
USB_P7_P8_OVC	PX1-B16	I/O	USB over current for ports 7 and 8	
USB_P4_P12_OVC	PX1-A26	I/O	USB over current for ports 4 and 12	
USB_P5_P13_OVC	PX1-A47	I/O	USB over current for ports 5 and 13	

5.4 SMBus

Table 8 SMBus Interface Signals

Signal Name	Pin #	Type	Description	Notes
SMBus-0				
SMBUS_P0_CLK	PX1-A14	I/OD	SMBus channel 0 clock	
SMBUS_P0_DAT	PX1-A15	I/OD	SMBus channel 0 data	
SMBus-2				
SMBUS_P2_CLK	PX2-A39	I/OD	SMBus channel 2 clock	
SMBUS_P2_DAT	PX2-A40	I/OD	SMBus channel 2 data	
SMBus thermal				
SMBUS_THRM_CLK	PX2-B39	I/O	APU temperature sensor SMBus clock	
SMBUS_THRM_DAT	PX2-B40	I/O	APU temperature sensor SMBus data	
SMBus generic				
SMBUS_ALERT#	PX1-A10	I/O	SMBus alert - this signal can be used to wake the system or generate an SMI	

5.5 Digital Audio

Table 9 Digital Audio Interface Signals

Signal Name	Pin #	Type	Description	Notes
HDA_ RST#	PX1-A16	O	HD audio interface reset	
HDA_SYNC	PX1-A17	O	HD audio sync signal to codec	
HDA_CLK	PX1-A18	O	HD audio interface bit clock	
HDA_SOUT	PX1-A19	O	HD audio serial data output to codec	
HDA_SIN1	PX1-A20	I/O	HD audio serial data input from a second codec	
HDA_SIN2	PX1-A21	I/O	HD audio serial data input from a third codec	

5.6 LPC

Table 10 LPC Interface Signals

Signal Name	Pin #	Type	Description	Notes
LPC_LAD0	PX1-A30	I/O	Multiplexed command / address / data bit 0	
LPC_LAD1	PX1-A31	I/O	Multiplexed command / address / data bit 1	
LPC_LAD2	PX1-A32	I/O	Multiplexed command / address / data bit 2	
LPC_LAD3	PX1-A33	I/O	Multiplexed command / address / data bit 3	
LPC_CLK	PX1-B23	O	33MHz clock for LPC device	
LPC_LFRAME#	PX1-B24	O	LPC bus frame	
LPC_SER_IRQ	PX1-B22	I/O	Serial IRQ	

5.7 GPIOs

Table 11 GPIO Signals

Signal Name	Pin #	Type	Description	Notes
FCH_GPIO0	PX2-B4	I/O	S0-domain General Purpose I/O	GPIO state is not preserved in sleep mode
FCH_GPIO1	PX2-B10			
FCH_GPIO3	PX2-B16			
FCH_GPIO4	PX2-B12			
FCH_GPIO5	PX2-B14			
FCH_GPIO6	PX2-B15			
FCH_GPIO7	PX2-B17			
FCH_GPIO8	PX2-B18			
FCH_GPIO9	PX2-B20			
FCH_GPIO10	PX2-B21			
FCH_GPIO11	PX2-B23			
FCH_GPIO12	PX2-B24			
FCH_GPIO54	PX1-A46			
FCH_GPIO57	PX2-A42			
FCH_GPIO58	PX2-A43			
FCH_GPIO182	PX1-A22	I/O	S5-domain General Purpose I/O	GPIO state is preserved in sleep mode
FCH_GPIO201	PX2-A20			
FCH_GPIO202	PX2-A21			
FCH_GPIO204	PX2-A23			
FCH_GPIO205	PX2-A24			
FCH_GPIO129_OD	PX2-A17	I/OD	General Purpose I/OD	GPIO state is not preserved in sleep mode
FCH_GPIO130_OD	PX2-A18			
FCH_GPIO144_OD	PX2-A14			
FCH_GPIO145_OD	PX2-A4			
FCH_GPIO146_OD	PX2-A10			
FCH_GPIO147_OD	PX2-A15			
FCH_GPIO149_OD	PX2-A16			
FCH_GPIO150_OD	PX2-A22			
FCH_PWM0_GPIO197	PX2-B44	I/O	S5-domain General Purpose I/O	GPIO state is preserved in sleep mode
FCH_PWM1_GPIO198	PX2-B47			

NOTE: GPIO numbering corresponds with GPIO numbering in the A55E controller hub documentation.

5.8 Power

Table 12 Power Signals

Signal Name	Pin #	Type	Description	Notes
GND	PX1-A1, PX1-B1, PX1-A7, PX1-A23, PX1-B25, PX1-A29, PX1-A34, PX1-A40, PX1-B40, PX2-A1, PX2-B1, PX2-A7, PX2-B7, PX2-A13, PX2-B13, PX2-A25, PX2-B25, PX2-A32, PX2-B32, PX2-A38, PX2-B41, PX2-A44, PX2-A50	P	Main GND rail	
5V_S5	PX1-B7, PX1-A13, PX1-B13, PX1-B19, PX2-A19, PX2-B19	P	S5-domain 5V power rail	
VCC_12V	PX1-A47, PX1-A48, PX1-A49, PX1-A50, PX1-B47, PX1-B48, PX1-B49, PX1-B50, PX2-B48, PX2-B49, PX2-B50	P	Main 12V power rail	

5.9 Miscellaneous

Table 13 Miscellaneous Signals

Signal Name	Pin #	Type	Description	Notes
FACE_PRSNT#	PX1-B34	I	FACE module presence detection. Must be connected to GND.	
PWR_BTN#	PX1-A43	I	Power button - causes an SMI or SCI to indicate a system request to enter a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWR_BTN# is asserted for more than 4 seconds, it will cause an unconditional transition (power button override) to the S5 state with only the PWR_BTN# available as a wake event. Override will occur even if the system is in the S1 state. This signal has an internal pull-up resistor.	
SLEEP_S3#	PX1-B43	O	S3 sleep power plane control. Assertion of SLP_S3# shuts off power to non-critical components when system transitions to S3, S4, or S5 states. De-assertion of SLP_S3# turns on power to non-critical components when system transitions from S3, S4, or S5 back to S0.	
RESERVED	PX1-A4, PX1-B2, PX1-B3, PX1-B5, PX1-B6, PX1-B10, PX1-B20, PX1-B20, PX1-B26, PX1-B27, PX1-B28, PX1-B29, PX1-B30, PX1-B37, PX1-B46, PX2-A2, PX2-A3, PX2-A5, PX2-A6, PX2-B2, PX2-B3, PX2-B5, PX2-B6, PX2-B28, PX2-B29, PX2-B30, PX2-B31, PX2-A35, PX2-B33, PX2-B34, PX2-B35, PX2-B36, PX2-B37, PX2-B38, PX2-B42, PX2-B43, PX2-B45, PX2-B46	-	Reserved for future use. Should be left unconnected.	
NC	PX2-A8, PX2-A9, PX2-A11, PX2-A12, PX2-B8, PX2-B9, PX2-B11, PX2-A26, PX2-A27, PX2-A28, PX2-A29, PX2-A30, PX2-A31, PX2-A33, PX2-A34, PX2-A36, PX2-A37	-	Should be left unconnected.	

6 CONNECTORS

6.1 HDMI Connector (P13)

The HDMI display output is provided through the standard HDMI socket (P13).

For additional details, please refer to section 3.3.1 of this document.

6.2 DisplayPort Connector (P19)

The DisplayPort display output is provided through the standard DisplayPort connector (P19).

For additional details, please refer to section 3.3.2 of this document.

6.3 DC Power Jack (J2)

DC power input connector.

Table 14 J2 connector pin-out

Pin	Signal Name
1	VIN_12V
2	GND

Table 15 J2 connector data

Manufacturer	Mfg. P/N
Contact Technology	DC-081HS

The connector is compatible with the Fit-PC3 power supply unit supplied by CompuLab.

6.4 RS232 connector (P2)

The Fit-PC3 RS232 port is routed to the on-board RS232 ultra-mini connector (P2). All signals are at RS232 levels.

Table 16 P2 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	RS232_TXD	5	RS232_DTR
2	RS232_RTS	6	RS232_DSR
3	RS232_RXD	7	RS232_RI
4	RS232_CTS	8	GND

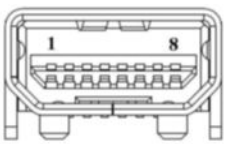


Table 17 P2 connector data

Manufacturer	Mfg. P/N	Mating connector
Wieson	G3169-500001	Wieson, P/N: 4306-5000

The connector is compatible with the serial cable adapter (CompuLab P/N 199D10230) supplied by CompuLab.

6.5 Audio Jacks (P5, P9)

The Fit-PC3 features two 3.5mm jacks. The analog audio signal pin-outs are compatible with standard 3-pole audio cables. The additional pins (S/PDIF output on P5 and S/PDIF input on P9) are accessible with the 3.5mm-to-RCA adapter cable (CompuLab P/N 199D10300) available from CompuLab.

Table 18 P5 connector pin-out

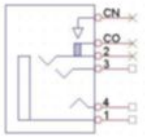
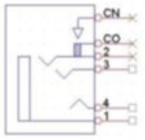
Pin	Signal Name	Jack pin-out	Mating plug
1	AUDIO_GND		
2	S/PDIF_OUT		
3	AUDIO_OUT_R		
4	AUDIO_OUT_L		
CO	SENSE_OUT		

Table 19 P9 connector pin-out

Pin	Signal Name	Jack pin-out	Mating plug
1	AUDIO_GND		
2	SPDIF_IN		
3	AUDIO_IN_R		
4	AUDIO_IN_L		
CO	SENSE_IN		

6.6 USB 3.0 Host Connectors (P8A, P8B)

The Fit-PC3 USB3.0 host ports are available through a dual-stacked USB 3.0 standard type-A connector (P8).

6.7 USB 2.0 Host Connectors (P11A, P11B)

The Fit-PC3 USB2.0 host ports are available through a dual-stacked USB 2.0 standard type-A connector (P11).

6.8 Gigabit Ethernet Connector (P12)

The Fit-PC3 Gigabit Ethernet port is routed to the standard RJ-45 connector (P12).

6.9 eSATA Connectors (P16A, P16B)

The Fit-PC3 eSATA ports are available through a dual-stacked standard eSATA connector (P16).

6.10 SATA Header (P3)

The SATA header (P3) is utilized for the Fit-PC3 internal SATA storage. The connector is not intended for external usage.

Table 20 P3 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	GND	7	GND
2	SATA_C_TX0_P	8	NC
3	SATA_C_TX0_N	9	VDD_5V
4	GND	10	VDD_5V
5	SATA_C_RX0_N	11	NC
6	SATA_C_RX0_P	12	NC

6.11 Front Panel Header (P6)

The front panel header (P6) is utilized for the Fit-PC3 internal front panel connection. The connector is not intended for external usage.

Table 21 P6 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	5V_S0	4	FCH_LED_PWM
2	IR_RX_FP	5	SATA_ACT#
3	3V3_S5	6	GND

6.12 Mini-PCIe sockets (P4, P7)

The Fit-PC3 features two standard mini-PCIe sockets – P4 and P7.

P4 is a standard full-size mini-PCIe socket. P7 is a standard half-size mini-PCIe socket.

6.13 SO-DIMM Sockets (P14, P18)

The Fit-PC3 features two standard DDR3 204-pin SO-DIMM sockets – P14 and P18.

6.14 FACE Extension Connectors (PX1, PX2)

Table 22 PX1 connector pin-out

Pin	Signal Name	Pin	Signal Name
A1	GND	B1	GND
A2	SATA_P2_TX_P	B2	RESERVED
A3	SATA_P2_TX_N	B3	RESERVED
A4	RESERVED	B4	SATA_ACT#
A5	SATA_P2_RX_P	B5	RESERVED
A6	SATA_P2_RX_N	B6	RESERVED
A7	GND	B7	5V_S5
A8	SATA_P3_TX_P	B8	SATA_P1_TX_P
A9	SATA_P3_TX_N	B9	SATA_P1_TX_N
A10	SMBALERT#	B10	RESERVED
A11	SATA_P3_RX_P	B11	SATA_P1_RX_P
A12	SATA_P3_RX_N	B12	SATA_P1_RX_N
A13	5V_S5	B13	5V_S5
A14	SMBUS_P0_CLK	B14	USB_P8_P
A15	SMBUS_P0_DAT	B15	USB_P8_N
A16	HDA_ RST#	B16	USB_P7_P8_OVC
A17	HDA_SYNC	B17	USB_P7_P
A18	HDA_CLK	B18	USB_P7_N
A19	HDA_SOUT	B19	5V_S5
A20	HDA_SIN1	B20	RESERVED
A21	HDA_SIN2	B21	RESERVED
A22	FCH_GPIO182	B22	LPC_IRQ
A23	GND	B23	LPC_CLK
A24	USB_P4_P	B24	LPC_LFRAME#
A25	USB_P4_N	B25	GND
A26	USB_P4_P12_OVC	B26	RESERVED
A27	USB_P12_P	B27	RESERVED
A28	USB_P12_N	B28	RESERVED
A29	GND	B29	RESERVED
A30	LPC_LAD0	B30	RESERVED
A31	LPC_LAD1	B31	PCIE_RESET#
A32	LPC_LAD2	B32	PCIE_CLK1_P
A33	LPC_LAD3	B33	PCIE_CLK1_N
A34	GND	B34	FACE_PRSNT#
A35	PCIE_P3_TX_P	B35	PCIE_P3_RX_P
A36	PCIE_P3_TX N	B36	PCIE_P3_RX_N
A37	PCIE_WKUP#	B37	RESERVED
A38	PCIE_P2_TX_P	B38	PCIE_P2_RX_P
A39	PCIE_P2_TX_N	B39	PCIE_P2_RX_N
A40	GND	B40	GND
A41	PCIE_P1_TX_P	B41	PCIE_P1_RX_P
A42	PCIE_P1_TX_N	B42	PCIE_P1_RX_N
A43	PWR_BTN#	B43	SLEEP_S3#
A44	PCIE_P0_TX_P	B44	PCIE_P0_RX P
A45	PCIE_P0_TX_N	B45	PCIE_P0_RX_N
A46	FCH_GPIO54	B46	RESERVED
A47	VCC_12V	B47	VCC_12V
A48	VCC_12V	B48	VCC_12V
A49	VCC_12V	B49	VCC_12V
A50	VCC_12V	B50	VCC_12V

Table 23 PX2 connector pin-out

Pin	Signal Name	Pin	Signal Name
A1	GND	B1	GND
A2	RESERVED	B2	RESERVED
A3	RESERVED	B3	PCIE_P2_TX_N
A4	FCH_GPIO145_OD	B4	FCH_GPIO0
A5	RESERVED	B5	RESERVED
A6	RESERVED	B6	RESERVED
A7	GND	B7	GND
A8	NC	B8	NC
A9	NC	B9	NC
A10	FCH_GPIO146_OD	B10	FCH_GPIO1
A11	NC	B11	NC
A12	NC	B12	FCH_GPIO4
A13	GND	B13	GND
A14	FCH_GPIO144_OD	B14	FCH_GPIO5
A15	FCH_GPIO147_OD	B15	FCH_GPIO6
A16	FCH_GPIO149_OD	B16	FCH_GPIO3
A17	FCH_GPIO129_OD	B17	FCH_GPIO7
A18	FCH_GPIO130_OD	B18	FCH_GPIO8
A19	5V_S5	B19	5V_S5
A20	FCH_GPIO201	B20	FCH_GPIO9
A21	FCH_GPIO202	B21	FCH_GPIO10
A22	FCH_GPIO150_OD	B22	NC
A23	FCH_GPIO204	B23	FCH_GPIO11
A24	FCH_GPIO205	B24	FCH_GPIO12
A25	GND	B25	GND
A26	NC	B26	PCIE_CLK2_P
A27	NC	B27	PCIE_CLK2_N
A28	NC	B28	RESERVED
A29	NC	B29	RESERVED
A30	NC	B30	RESERVED
A31	NC	B31	RESERVED
A32	GND	B32	GND
A33	NC	B33	RESERVED
A34	NC	B34	RESERVED
A35	RESERVED	B35	RESERVED
A36	NC	B36	RESERVED
A37	NC	B37	RESERVED
A38	GND	B38	RESERVED
A39	SMBUS_P2_CLK	B39	SMBUS_THRM_CLK
A40	SMBUS_P2_DAT	B40	SMBUS_THRM_DAT
A41	PCIE_CLKREQ#	B41	GND
A42	FCH_GPIO57	B42	RESERVED
A43	FCH_GPIO58	B43	RESERVED
A44	GND	B44	FCH_PWM0_GPIO197
A45	USB_P13_P	B45	RESERVED
A46	USB_P13_N	B46	RESERVED
A47	USB_P5_P13_OVC	B47	FCH_PWM1_GPIO198
A48	USB_P5_P	B48	VCC_12V
A49	USB_P5_N	B49	VCC_12V
A50	GND	B50	VCC_12V

Table 24 PX1, PX2 connector data

Manufacturer	Mfg. P/N	Mating connector
FCI	61082-10260[2|6]LF	61083-10460[2|6]LF

6.15 Power Button (SW2)

The Fit-PC3 power button SW2 controls the system power state. For additional details, please refer to section 4.1.3 of this document.

7 MECHANICAL DRAWINGS

The mechanical drawings below are provided for connector location information.

Full mechanical drawings are available at http://www.fit-pc.com/.

Figure 2 Fit-PC3 mother-board top

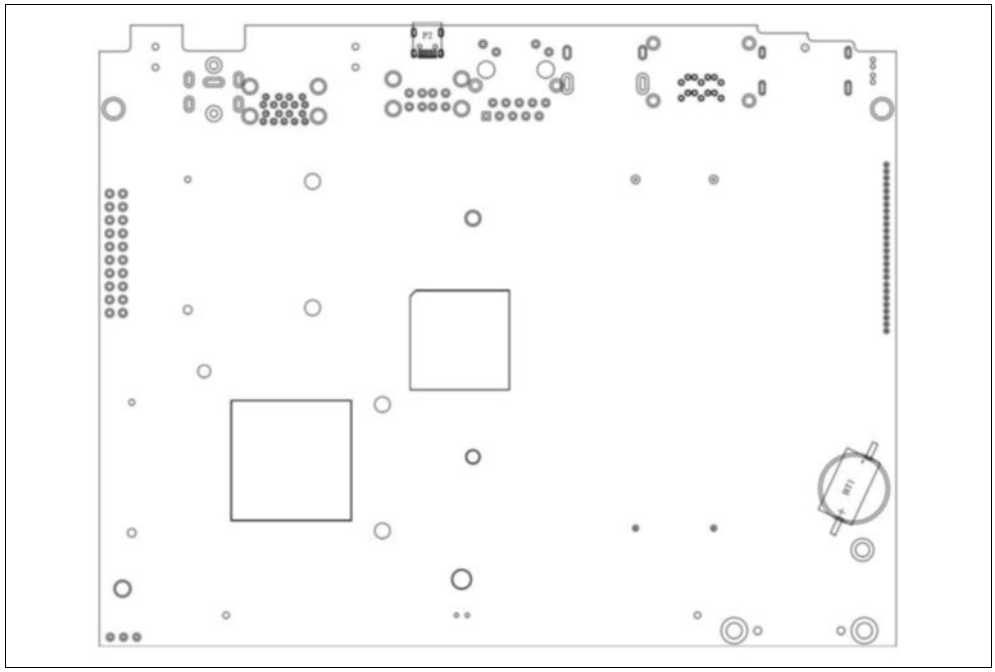
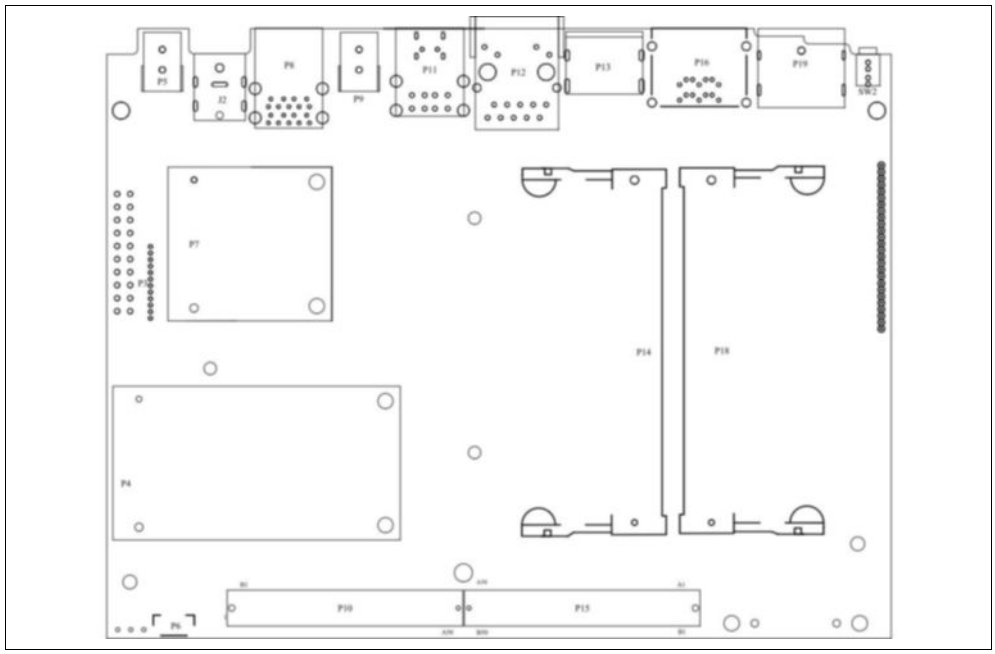


Figure 3 Fit-PC3 mother-board bottom (x-ray view - as seen from top side)



8 CUSTOM FACE MODULE DESIGN

The fit-PC3 has been designed to allow integration of custom FACE (Function And Connectivity Extension) modules.

Please refer to the “FACE module design guide” application note and to the “FACE module design package” available at http://www.fit-pc.com/.

9 OPERATIONAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

Table 25 Absolute Maximum Ratings

Parameter	Min	Typ.	Max	Unit
Main power supply voltage	-0.3	12	18	V

NOTE: Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device.

9.2 Recommended Operating Conditions

Table 26 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage	10	12	16	V

9.3 DC Electrical Characteristics

Table 27 DC Electrical Characteristics

Parameter	Operating Conditions	Min	Typ	Max	Unit
3.3V Digital I/O					
V_{IH}		2.475		3.6	V
V_{IL}		-0.5		0.8	V
V_{OH}		2.8			V
V_{OL}				0.5	V
Open drain with internal pull up to 3.3V					
V_{IH}		2.3		3.8	V
V_{IL}		-0.5		1.0	V
V_{OL}	IOL = 3 mA	-		0.4	V
RS232					
TX Voltage Swing		±5	±5.4		V
RX Voltage Swing			±25		V